What is claimed is:

1. A method for fabricating a trench capacitor with an insulation collar in a substrate, which is electrically connected to the substrate on one side via a buried contact, having a planar selection transistor which is provided in the substrate and is connected via the buried contact, comprising:

providing a trench in the substrate using a hard mask with a corresponding mask opening;

providing a capacitor dielectric in a lower and central trench region, the insulation collar in the central and upper trench region and an electrically conductive filling in the lower, central and upper trench region, a top side of the electrically conductive filling being sunk in the upper trench region with respect to the top side of the substrate;

providing at least one liner on the hard mask and in the trench;

carrying out an oblique implantation of impurity ions into the trench using the hard mask for altering the properties of a partial region of a topmost liner;

forming a liner mask from the partial region or the complementary partial region of the topmost liner for defining a contact region on one side and an insulation region on a different side of the buried contact; and

completing the connection region on the one side and the insulation region on the different side of the buried contact by removing and replacing a part of the filling and/or a part of the insulation collar using the liner mask.

2. The method according to claim 1, wherein the conductive filling has a region which fills the trench above the insulation collar and from which a partial region is removed using the mask and is subsequently filled with an insulating filling to complete the insulation region.

3. The method according to claim 1, wherein a lower liner made of silicon nitride and an upper liner made of undoped polysilicon or amorphous silicon are provided and the implantation introduces boron ions into the partial region, whereupon the complementary partial region is removed by selective etching.

4. The method according to claim 3, wherein the partial region is converted into an oxidized partial region after the selective etching by oxidation, by means of which oxidized partial region, as a mask, the lower liner made of silicon nitride and the part of the filling are removed by selective etching.

5. The method according to claim 1, wherein a liner made of undoped polysilicon or amorphous silicon is provided and the implantation introduces nitrogen ions into the partial region, whereupon the complementary partial region is selectively oxidized and then selectively removed by etching.

6. The method according to claim 5, wherein, by the liner mask, a part of the insulation collar is removed by selective etching and subsequently filled with a conductive filling for forming the contact region.

7. The method according to claim 1, wherein a liner made of undoped polysilicon or amorphous silicon is provided and the implantation introduces boron ions into the partial region, whereupon the complementary partial region is selectively removed by etching.

8. The method according to claim 7, wherein, by the liner mask, a part of the insulation collar is removed by selective etching and subsequently filled with a conductive filling for forming the contact region.

9. The method according to claim 1, wherein a lower liner made of silicon oxynitride and an upper liner made of undoped polysilicon or amorphous silicon are provided and the implantation introduces nitrogen ions into the partial region, whereupon the complementary partial region is oxidized and then the partial region and an underlying region of the lower liner and is selectively removed by etching.

10. The method according to claim 9, wherein, by the liner mask, a part of the insulation collar is removed by selective etching and subsequently filled with a conductive filling for forming the contact region.

11. The method according to claim 1, wherein laterally in the upper region of the trench on the semiconductor substrate, regions made of oxynitride are provided, a liner made of undoped polysilicon or amorphous silicon is provided and the implantation introduces boron ions into the partial region, whereupon the complementary partial region is selectively removed by etching.

12. The method according to claim 11, wherein the insulation collar is provided outside the trench in the surface of the semiconductor substrate and the conductive filling is sunk deeper than the insulation collar, and after the removal of the region made of oxynitride in the contact region, is filled with a conductive filling for forming the contact region.

13. A method for fabricating a trench capacitor with an insulation collar in a substrate, which is electrically

connected to the substrate on one side via a buried contact, having a planar selection transistor which is provided in the substrate and is connected via the buried contact, comprising:

providing a trench in the substrate using a hard mask with a corresponding mask opening;

providing a capacitor dielectric in a lower and central trench region, the insulation collar in a central and upper trench region and an electrically conductive filling in the lower, central and upper trench region, a top side of the electrically conductive filling being sunk in the upper trench region with respect to a top side of the substrate;

lowering the insulation collar to below the top side of the conductive filling;

providing an etching stop layer in the trench;

providing a spacer in the trench;

carrying out an oblique implantation of impurity ions into the trench using the hard mask for altering the properties of a partial region of the spacer;

forming a spacer mask from the partial region of the spacer for defining a contact region on one side and an insulation region on a different side of the buried contact; and

completing the connection region on the one side and the insulation region on the different side of the buried contact by successively removing the other partial region of the spacer and filling with an insulating filling and removing the partial region of the spacer and the etching stop layer and filling with a conductive filling.

14. A method for fabricating a trench capacitor with an insulation collar in a substrate, which is electrically connected to the substrate on one side via a buried contact, having a planar selection transistor which is provided in the substrate and is connected via the buried contact, comprising:

providing a trench in the substrate using a hard mask with a corresponding mask opening;

providing a capacitor dielectric in a lower and central trench region, the insulation collar in the central and upper trench region and an electrically conductive filling in the lower, central and upper trench region, a top side of the electrically conductive filling being sunk in the upper trench region with respect to a top side of the substrate;

lowering the insulation collar to below the top side of the conductive filling;

providing an etching stop layer in the trench;

providing a spacer in the trench;

forming a mask and removing a partial region of the spacer by the mask for defining a contact region on one side and an insulation region on a different side of the buried contact; and

completing the connection region on one side and the insulation region on the different side of the buried contact by successively removing the other partial region of the spacer and filling with an insulating filling and removing the partial region of the spacer and the etching stop layer and filling with a conductive filling.

15. The method according to claim 13, wherein a step of widening the mask opening and the upper region of the trench and of narrowing the top side of the conductive filling is carried out.

16. The method according to claim 14, wherein the partial region and the other partial region of the spacer are separated from one another by an etching step for forming parallel isolation trenches and the impurity ions are subsequently diffused out in the partial region.